ABSTRACT OF THE DISCLOSURE

In a digital filter of a DPLL (digital phase locked loop) for minimizing the bit error rate for multiple communications protocols, a first reloadable register portion stores a TBW (total bandwidth) value programmed into the first reloadable register portion through a first port, and a second reloadable register portion stores a DBW (differential bandwidth) value programmed into the second reloadable register portion through a second port. An up_counter generates an UP_CNT value by counting up each UP signal pulse generated by a phase transition detector when a first phase of a SDIN (serial data input) signal leads a second phase of a current ACLK (recovered clock) signal. A down_counter generates a DOWN_CNT value by counting up each DOWN signal pulse generated by the phase transition detector when the first phase of the SDIN (serial data input) signal lags the second phase of the current ACLK (recovered clock) signal. One of a FWD (forward) signal or a BWD (backward) signal are asserted or are both not asserted depending on the UP_CNT value and the DN_CNT value in comparison to the TBW value and the DBW value. Another clock signal having a leading phase from the current ACLK signal is selected as a new ACLK (recovered clock) signal when the FWD signal is asserted. Or, another clock signal having a lagging phase from the current ACLK signal is selected as the new ACLK (recovered clock) signal when the BWD signal is asserted. Or, the current ACLK signal remains as the new ACLK (recovered clock) signal if neither the FWD signal nor the BWD signal is asserted.